Syllabus

for

Master of Technology- 1st Year

(Electronics & Communication Engineering)

w.e.f.

2021-22

Department of Electronics & Communication Engg.

Guru Jambheshwar University of Science & Technology
HISAR

INDEX

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M.Tech (ECE)

Program Outcomes and Program Specific Outcomes

PO1: An ability to independently carry out research /investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PSO1: Students should be able to develop advanced understanding of the concepts of Electronics & communication engineering and their applications in the specific areas of VLSI, Communication Engineering and signal processing.

PSO2: Students should have an ability to apply technical knowledge of modern hardware & software tools for the design of electronic subsystems for solving various engineering problems.

Semester	Total Credits
I	26
II	22
III	14
IV	08
Total	70

- 04 contact hours per week are required for each theory subject including electives. However, 03 contact hours per week are required for open elective subject.
- 04 contact hours per week are required for each laboratory course.
- 02 hrs per student per week teaching load will be assigned to supervisor for thesis work for Part I and Part II each.

M. Tech. (ECE), 1st semester							
Sr. No.	Course Code	Course Title	Teaching Schedule (Hrs/week)			Credit	Exam Duration (Hr)
			L	T	P		
1	ECL-712	IC Fabrication Technology	4	0	0	4	3
2	ECL-713	Digital VLSI Design	4	0	0	4	3
3	ECL-714	Hardware Description Language	4	0	0	4	3
4	ECL-715	Embedded System Design	4	0	0	4	3
5	ECL-719	Signal Processing	4	0	0	4	3
6	ECP-716	Digital VLSI Design Lab	0	0	4	2	3
7	ECP-717	Hardware Description Language Lab	0	0	4	2	3
8	ECP-718	Embedded System Design Lab	0	0	4	2	3
9		Audit Course*	2	0	0	0	3
		Total	**22**	**0**	**12**	**26**	

*List of Audit course (1st Semester)

The student can opt for any one subject from the following list.

Sr. No.	Course Code	Course Title
1	AC01	English For Research Paper Writing
2	AC02	Disaster Management
3	AC04	Value Education
4	AC07	Stress Management By Yoga

M. Tech. (ECE), 2nd semester							
Sr. No.	**Course Code**	**Course Title**	**Teaching Schedule (Hrs/week)**			**Credit**	**Exam Duration (Hr)**
			L	**T**	**P**		
1	ECL-721	Mobile Communication	4	0	0	4	3
2	ECL-722	Advance Optical Communication System	4	0	0	4	3
3	ECL-723	Analog IC Design	4	0	0	4	3
4	ECL-724	Adaptive Signal Processing	4	0	0	4	3
5	ECL-725	Elective-I*	4	0	0	4	3
6	ECP-726	Adaptive Signal Processing Lab	0	0	4	2	3
7		Audit Course*	2	2	2	2	3
		Total	**22**	**0**	**04**	**22**	

*List of Elective-I (2nd Semester)

The student can opt for any one subject from the following list.

Sr. No.	Course Code	Course Title
1	ECL-725(i)	Algorithm for VLSI Design Automation
2	ECL-725(ii)	Advanced Computer Architectures
3	ECL-725(iii)	MEMS and IC Integration

*List of Audit course (2nd Semester)

The student can opt for any one subject from the following list.

Sr. No.	Course Code	Course Title
1	AC03	Sanskrit For Technical Knowledge
2	AC05	Constitution of India
3	AC06	Pedagogy Studies
4	AC08	Personality Development through Life Enlightenment Skills

First Semester

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective	Credit	L	P
ECL-712	IC Fabrication Technology	Core	4	4	0

Max Marks: 100 (Internal: 30, External: 70)

Course Assessment Methods: Both Continuous & Semester End Assessment

Pre-requisites: Analog electronics, VLSI design

Course Objectives: This is the very first course for the post-graduate students. This course first gives the knowledge of the necessary environment conditions for the integration technology. All the fabrication processes are then discussed step-by step which includes wafer cleaning, wet etching, ion implantation, oxidation, lithography, chemical vapour deposition, metal film deposition, etching and then safe packaging.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able to	RBT Level
CO1	**Define & describe** basic terminology related to IC fabrication process.	LOTS: Level 1 Remember
CO2	**Explain** various techniques such as oxidation, lithography, CVD technique etc.	LOTS: Level 2 Understand
CO3	**Apply** knowledge of lithography, metallization and packing for ICs.	LOTS: Level 3 Apply
CO4	**Compare & evaluate** the lithography procedure and advanced lithography techniques used in the industry.	HOTS: Level 4 & 5 Analyze & evaluate
CO5	**Design** integrated circuits in a better fashion with thorough knowledge of IC fabrication technique.	HOTS: Level 6 Create

UNIT-1

Environment for VLSI Technology: Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques.

Impurity incorporation: Solid State diffusion modelling and technology; Ion Implantation modelling, technology and damage annealing; characterization of Impurity profiles.

UNIT-2

Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI; Characterizations of oxide films; High k and low k dielectrics for ULSI.

Lithography: Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation.

UNIT-3

Chemical Vapour Deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modelling and technology.

Metal film deposition: Evaporation and sputtering techniques. Failure mechanisms in metal interconnects; Multi-level metallization schemes.

UNIT-4

Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI. Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technology.

Texts/References Books:

1. S.K. Gandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1994(2nd Edition).
2. S.M. Sze (Ed), VLSI Technology, 2nd Edition, McGraw Hill, 1988.
3. Plummer, Deal, Griffin "Silicon VLSI Technology: Fundamentals, Practice & Modeling"PH, 2001.
4. P. VanZant, "Microchip Fabrication", 5th Edition, MH, 2000.

Note: The Examiner will set nine questions. First question will be compulsory, covering the entire syllabus. Apart from Question No. 1, rest of the paper will consist of four units as per the syllabus taking two questions from each unit. However, student may be asked to attempt only 1 question from each unit. All questions will carry equal marks.

Course Articulation Matrix:

IC Fabrication Technology (ECL-712)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	L	--	M	H	M
CO 2	H	--	M	H	H
CO 3	L	L	H	H	H
CO 4	L	--	M	H	H
CO 5	H	--	H	M	H

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Max Marks: 100 (Internal: 30, External: 70)

Course code	Title of course	Core/Elective	Credit	L	P
ECL-713	Digital VLSI Design	Core	4	4	0

Course Assessment Methods: Both Continuous & Semester End Assessment

Pre-requisites: Digital Electronics

Course Objectives: This course is intended to be used for the first year post- graduate students. This course aims at covering first the basic building block of the VLSI circuits, that is, MOSFET and then the design equations for MOS, transistor sizing, various logic circuits design using MOS transistor. Memory designs and layouts are also covered under this course.

Course Outcomes:

Sr. No.	At end of the semester, student will be able to	RBT Level
CO-1	**Describe** CMOS circuits and systems and their technical specifications and uses.	LOTS: Level 1 Remember
CO-2	**Understand** various CMOS technologies for logic gates, circuits and systems.	LOTS: Level 2 Understand
CO-3	**Apply** the concepts of CMOS logics for the design of digital integrated circuits and systems.	LOTS: Level 3 Apply
CO-4	**Analyze & evaluate** CMOS static and dynamic circuits and systems.	HOTS: Level 4 & 5 Analyze & evaluate
CO-5	**Design and describe** CMOS circuits and systems for digital IC design, test and verification.	HOTS: Level 6 Create

UNIT-1

Introduction to CMOS Technology: brief history, MOS transistors and switches, Design partitioning, Circuit and system representations examples, Design abstractions, design verification and testing. Technology related CAD issues. CMOS processing Technology- brief overview, CMOS technologies, Latch-up

UNIT- 2

MOS transistor theory: introduction, depletion and enhancement MOS transistor, MOS device design equations, current voltage (I-V) characteristics, Capacitance voltage (C-V) characteristics, second order effects, MOS models and small signal characteristics, Body Effect. CMOS inverter DC characteristics, static load MOS inverters, enhancement load versus depletion load inverter, CMOS inverter switching characteristics, power dissipation, charge sharing. Scaling of MOS transistors

UNIT- 3

CMOS logic gate design, logic fan-in, fan-out characteristics, Noise Margin, inverter device sizing, CMOS circuits-Combinational MOS Logic Circuits: Pass Transistors/Transmission Gates; Designing with transmission gates, Primitive Logic Gates; Complex Logic Circuits. Sequential MOS Logic Circuits: SR Latch, clocked Latch and flip flop circuits, CMOS D latch and edge triggered flip flop, set up and hold time, two phase clocking, clock distribution.

UNIT- 4

CMOS logic structures-CMOS complementary logic, pseudo – nMOS logic, dynamic logic, Clocked CMOS logic, CMOS domino logic, NP domino logic, cascade voltage switch logic, memory elements, Finite state machines, CMOS testing- need, principles and design strategies for test-brief introduction.

Text books:

1. Neil H. E. Weste, K. Eshraghian. Principles of CMOS VLSI Design: A Systems Perspective. Second Edition (Expanded), AW/Pearson, 2001.
2. Neil H. E. Weste and David M Harris, CMOS VLSI Design: A Circuits and systems Perspective. Fourth Edition, AW/Pearson, 2011.

Reference books:

1. S. M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, Third Edition, MH, 2002.
2. J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, Digital Integrated Circuits: A DesignPerspective, Second Edition, PH/Pearson, 2003.
3. D. A. Pucknell and K. Eshraghian, Basic VLSI Design: Systems and Circuits, Third Edition, PHI. 1994.
4. J. P. Uyemura, CMOS Logic Circuit Design, Kluwer, 1999.
5. J. P. Uyemura, Introduction to VLSI Circuits and System, Wiley, 2002.
6. R. J. Baker, H. W. Li and D. E. Boyce, CMOS Circuit Design, Layout and Simulation, PH, 1997.

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Course Articulation Matrix:

Digital VLSI Design (ECL-713)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	H	H	H	H	H
CO 2	H	H	H	H	M
CO 3	M	H	H	H	M
CO 4	M	H	M	H	M
CO 5	H	H	H	H	M

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective	Credit	L	P
ECL-714	Hardware Description Language	Core	4	4	0

Max Marks: 100 (Internal: 30, External: 70)

Course Assessment Methods: Both Continuous & Semester End Assessment

Pre-requisites: Digital Electronics

Course Objective: This course is for first year post graduation students. This course is designed to make students learn popular hardware descriptive languages such as Verilog & VHDL. The course begins with the introduction of Hardware design and Design Methodologies. Basic and advanced concepts required to write a Verilog code are covered in detail.

Course outcomes:

Sr. No.	At end of the semester, student will be able to	RBT Level
CO-1	**Describe** the digital circuits and systems in Verilog with specifications for different applications.	LOTS: Level 1 Remember
CO-2	**Understand** behavioural, dataflow and Gate level modelling for digital logics and system implementation, testing of digital logic.	LOTS: Level 2 Understand
CO-3	**Apply** the concepts of Verilog HDL for digital logics design, synthesis, test and verification.	LOTS: Level 3 Apply
CO-4	**Analyze & evaluate** the behaviour of digital circuits and systems using verilog.	HOTS: Level 4 & 5 Analyze & evaluate
CO-5	**Design** different digital circuits and systems for digital IC design, test and verification with Verilog.	HOTS: Level 6 Create

UNIT-1

Digital system design automation with Verilog, digital design flow, Verilog HDL, Hierarchical Modeling Concepts,RTL design with Verilog, RTL level design, elements of Verilog, component description in Verilog, testbench, Verilog language concepts, characterizing hardware, module basics, Verilog simulation model, compiler directives, system tasks and functions

UNIT- 2

Combinational circuits description, module wire, gate level logic, hierarchical structure, assignment statements, behavioral combinational description, combinational synthesis

UNIT- 3

Sequential circuits description, sequential models, memory components, functional registers, state machines, sequential synthesis, Component test and verification, test bench, test bench techniques, design verification, assertion verification

UNIT- 4

Sequential multiplier, computer model, processor and memory model, data path part, control part, adding CPU Verilog description, CPU design and test

Text books:

1. Z. Navabi, Verilog Digital System Design, 2nd Edition, 2006, McGraw Hill
2. Samir Palnitkar, Verilog HDL-A Guide to Digital Design and Synthesis, 2001

Note: The Examiner will set nine questions. First question will be compulsory, covering the entire syllabus. Apart from Question No. 1, rest of the paper will consist of four units as per the syllabus taking two questions from each unit. However, student may be asked to attempt only 1 question from each unit. All questions will carry equal marks.

Course Articulation Matrix:

Hardware Description Language (ECL-714)					
	PO 1	PO 2	PO 3	PSO 1	PSO 2
CO 1	M	H	H	H	H
CO 2	H	H	H	H	H
CO 3	M	H	H	H	H
CO 4	M	H	M	H	M
CO 5	H	H	M	H	M

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective	Credit	L	P
ECL-715	Embedded System Design	Core	4	4	0

Max Marks: 100 (Internal: 30, External: 70)

Course Assessment Methods: Both Continuous & Semester End Assessment

Pre-requisites: Microprocessor, Basic of C language, Analog & Digital circuits

Course Objectives:

This course is designed to impart in-depth knowledge related to the architecture and programming of PIC micro-controller. The course provides thorough coverage to advanced and state-of-the-art ARM based micro-controllers. Further it also familiarizes students with the concepts and techniques of embedded system project management.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able:	RBT Level
CO 1	**Outline** the architecture of PIC & ARM microcontroller.	LOTS: Level 1 Remember
CO 2	**Explain** various kinds of instruction sets of PIC & ARM microcontroller.	LOTS: Level 2 Understand
CO 3	**Apply** knowledge of architecture & instruction set in writing assembly language programs.	LOTS: Level 3 Apply
CO 4	**Analyze** & evaluate various microcontroller based circuits.	HOTS: Level 4 & 5 Analyze & evaluate
CO 5	**Design and develop** an embedded system for different applications.	HOTS: Level 6 Create

UNIT 1

Introduction to PIC Microcontrollers: Comparison between PIC16 (mid range 8 bits family) and PIC18 (advanced 8 bits family) families of microcontrollers.

PIC Architecture: Pin Diagram, Functional Block diagram, Program Memory Organization, Special Function Registers and Data Memory Organization, Architecture of Instructions: Bit oriented, Byte oriented, Literal and Control instructions.

UNIT 2

Timers & Interrupts in PIC: Timer 0 Module, Timer 0 as counter; Block Diagram of Timer1 Module; Timer1 as synchronous and Asynchronous counter; Timer1 Oscillator; Block Diagram of Timer2 Module; Interrupt logic diagram, Timer0 Interrupt, Port-B change Interrupt, RB0 Interrupt; Timer1 and Timer2 Interrupts and External interrupts, Interrupt Service Routine

Instruction set in PIC: Assembly Language Programming Style and Instruction set (PIC 16F877A), Introduction to IDEs for PIC programming, Simple Arithmetic operations; TRIS Registers of PORT A, B, C, D and E.

UNIT 3

ARM Architecture: The Acorn RISC Machine, Architectural inheritance, The ARM programmer's model, and ARM development tools.
ARM architecture variants, 3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface.

UNIT 4

Instruction Set of ARM: Introduction, Exceptions, Conditional execution , Branch and Branch with Link (B, BL), Branch with Link and exchange (BX, BLX), Software Interrupt (SWI), Multiply instructions, Count leading zeros (CLZ - architecture v5T only), Single word and unsigned byte instructions, Half-word and signed byte instructions, Multiple register transfer instructions, Swap memory and register instructions (SWP), Status register to general register transfer instructions, General register to status register transfer instructions.

Text Books:

1. Design with PIC Microcontroller, by John B. Peatman, Pearson.
2. ARM System-on-Chip Architecture, by Steve Furber, PEARSON.

Reference Books:

1. PIC Microcontroller and Embedded Systems: using assembly and C for PIC 18, by Muhammad Ali Mazidi, Pearson.
2. ARM Assembly Language Programming & Architecture by Muhammad Ali Mazidi, Sarmad Naimi, SepehrNaimi, Shujen Chen, MicroDigitaEd.com

Note: The Examiner will set nine questions. First question will be compulsory, covering the entire syllabus. Apart from Question No. 1, rest of the paper will consist of four units as per the syllabus taking two questions from each unit. However, student may be asked to attempt only 1 question from each unit. All questions will carry equal marks.

Course Articulation Matrix:

Embedded System Design (ECL-715)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	H	--	M	H	M
CO 2	M	--	H	H	H
CO 3	H	L	H	H	H
CO 4	H	--	H	H	M
CO 5	H	M	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective	Credit	L	P
ECL-719	Signal Processing	Core	4	4	0

Max Marks: 100 (Internal: 30, External: 70)

Course Assessment Methods: Both Continuous & Semester End Assessment
Pre-requisites: Signal & System, Engineering Mathematics.

Course Objectives:

To introduce the concepts and techniques associated with the understanding of signal processing. To familiarize with techniques suitable for auditory perception and time delay estimation. To provide with an appreciation of applications for system modeling and identification.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able to:	RBT Level
CO-1	**Define & Describe** the terminologies used in speech processing.	LOTS: Level 1 Remember
CO-2	**Understand & explain** various models for analysis of speech and audio signal	LOTS: Level 2 Understand
CO-3	**Apply** signal theory for the channel equalization, estimation	LOTS: Level 3 Apply
CO-4	**Analyze & evaluate** various equalization and TDE techniques in signal processing.	HOTS: Level 4 & 5 Analyze & evaluate
CO-5	**Design** various system and identify various models for Speech, TDE, Equalization And DOA	HOTS: Level 6 Create

UNIT-1

Speech and Audio Processing: Speech communication acoustic theory of speech: the source–filter model speech models and features. linear prediction models of speech harmonic plus noise model of speech fundamental frequency (pitch) information, speech coding, speech recognition, basic audio processing, hearing, psychoacoustics of hearing, speech analysis and classification, role of LPC coefficients in analysis filter. LPC stability issues.

UNIT-2

Time Delay Estimation: Need for the time delay estimation, system model, source localization strategies, ideal model-free field environment, TDE methods: cross-correlation function (CCF) method, least mean square (LMS) adaptive filter method, average square difference function (ASDF) method.

UNIT-3

Bayesian Inference and Channel Equalization:, Bayesian inference,basic definition,Bayesian theorem,elements of Bayesian inference,dynamics and probability model inestimation,parameter estimation and signal restoration,ML and MAP estimation, Introduction and need For Channel Equalization, Types of Equalization Techniques.

UNIT-4

System modeling and DOA: System identification based on FIR (MA), All Pole (AR), Pole Zero (ARMA) system models, Basic Principle of DOA Estimation, Need of DOA, Beamforming, Direction of Arrival (DOA), Estimation Algorithms.

Text Books:

1. Simon S Haykins, "Adaptive Filter Theory"PHI, 3rd Edition
2. Proakis,"Digital Signal Processing"PHI 2nd edition

Note: The Examiner will set nine questions. First question will be compulsory, covering the entire syllabus. Apart from Question No. 1, rest of the paper will consist of four units as per the syllabus taking two questions from each unit. However, student may be asked to attempt only 1 question from each unit. All questions will carry equal marks.

Course Articulation Matrix:

Signal Processing (ECL-719)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	M	--	H	H	H
CO 2	H	--	H	H	H
CO 3	H	L	M	H	H
CO 4	**H**	**L**	**H**	**H**	**H**
CO 5	H	M	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective	Credit	L	P
ECP-716	Digital VLSI Design Lab	Core	2	0	4

Max Marks: 100 (Internal: 30, External: 70)

Course Assessment Methods: Both Continuous & Semester End Assessment

Pre-requisites: Digital Electronics, knowledge of various ICs

Course Objectives:

This course aims at covering first the basic building block of the VLSI circuits, that is, start with MOSFET characteristics and then go through various logic circuits design using MOS transistors (like CMOS inverter, NAND NOR, MUX, DFF, Register) to complete Memory designs and layouts are also covered under this course.

Course Outcomes:

Sr. No.	At end of the semester, Student will be able to	RBT Level
CO-1	**Understand software** tools and apply these tools for the realisation of VLSI logic gates, circuits and systems.	LOTS: Levels 3 Apply
CO-2	**Analyze and compare** the outcomes of different experimental models.	HOTS: Level 4 Analyse
CO-3	**Evaluate** the performance of designed CMOS static & dynamic circuits and systems.	HOTS: Level 5 Evaluate
CO-4	**Integrate** knowledge of different CMOS circuits and systems for digital IC design.	HOTS: Level 6 Create
CO-5	**Create** written records for the given experiments with problem definition, solution, observations & conclusion.	HOTS: Level 6 Create
CO-6	**Demonstrate** ethical practices while performing lab experiments individually or in the group.	LOTS: Level 3 Apply

List of Experiments

1. To study the characteristics of MOS Device.
2. To design and simulate the CMOS Inverter Characteristics
3. To design and simulate the CMOS NAND gate
4. To design and simulate the CMOS NOR gate
5. To design and simulate the CMOS XOR gate

6. To design and simulate the CMOS Multiplexer
7. To design and simulate the CMOS SR Latch
8. To design and simulate the CMOS D-FF
9. To design and simulate the CMOS 1-bit Full Adder
10. To design and simulate the CMOS SRAM

Note: Students are required to perform eight to ten experiments in the semester. The above list is an indicative list of experiments, which can be expanded by course coordinator depending on the course requirement.

Course Articulation Matrix:

Digital VLSI Design Lab (ECP-716)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	H	M	H	H	H
CO 2	H	M	H	H	H
CO 3	H	M	H	H	H
CO 4	H	M	M	H	M
CO 5	L	H	L	L	L
CO 6	H	M	--	--	--

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective	Credit	L	P
ECP-717	Hardware Description Language Lab	Core	2	0	4

Max Marks: 100 (Internal: 30, External: 70)

Course Assessment Methods: Both Continuous & Semester End Assessment

Pre-requisites: Digital Electronics

Course Objective:

This course is for first year post graduation students. This course is designed to give students in hand practice of writing and simulating a Verilog code which is one of the popular hardware descriptive language. Various combinational and sequential circuits like simple logic gates, Half Adder, Full Adder, Multiplexer, Demultiplexer, Encoder, decoder, Flip-Flops, Shift Register, Counters are included.

Course Outcomes:

Sr. No.	At end of the semester, student will be able to	RBT Level
CO-1	**Understand software** tools and apply these tools for the modelling styles of Verilog HDL for logic, gates, circuits and systems design.	LOTS: Levels 3 Apply
CO-2	**Analyze and compare** the outcomes of different experimental models.	HOTS: Level 4 Analyse
CO-3	**Evaluate** the performance of logics design and verification of digital integrated circuits and systems.	HOTS: Level 5 Evaluate
CO-4	**Integrate** knowledge for design of digital circuits and systems for VLSI design, test and verification.	HOTS: Level 6 Create
CO-5	**Create** written records for the given experiments with problem definition, solution, observations & conclusion.	HOTS: Level 6 Create
CO-6	**Demonstrate** ethical practices while performing lab experiments individually or in the group.	LOTS: Level 3 Apply

List of Experiments:

1. To design a Multiplexer Using Basic Gates in Verilog.
2. To design and describe a full adder in Verilog.
3. To design and describe an 8-bit ALU in Verilog.

4. To design and describe majority circuit in Verilog.
5. To design and describe latch and Flip-Flop in Verilog.
6. To design and describe D Type Flip-Flop with Synchronous and asynchronous Control in Verilog.
7. To design and describe a counter in Verilog.
8. To design and describe 8-bit universal shift register in Verilog.
9. To design and describe sequence detector in Verilog.
10. To implement any three design (given above) on FPGA kit.

Note: Students are required to perform eight to ten experiments in the semester. The above list is an indicative list of experiments, which can be expanded by course coordinator depending on the course requirement.

Course Articulation Matrix:

Hardware Description Language Lab (ECP-717)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	H	M	H	H	H
CO 2	H	M	H	H	H
CO 3	H	M	H	H	H
CO 4	H	M	M	H	M
CO 5	L	H	L	L	L
CO 6	H	M	--	--	--

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective	Credit	L	P
ECP-718	Embedded System Design Lab	Core	2	0	4

Max Marks: 100 (Internal: 30, External: 70)

Course Assessment Methods: Both Continuous & Semester End Assessment

Pre-requisites: C languages & basic of digital and analog circuits

Course Objectives:

The course is designed to provide hand-on experience to the students on the industry standard MP lab, KEIL make embedded Development boards related to PIC, ARM7 etc. processors. It provides students an opportunity to understand the architecture of latest micro-controllers through programming using KEIL software and development boards. The course familiarizes students with the interfacing of various application boards with development boards.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able:	RBT Level
CO 1	**Understand software** tools and apply these tools to write a program for microcontroller based applications.	LOTS: Levels 3 Apply
CO 2	**Analyze and compare** the outcomes of different experimental programs.	HOTS: Level 4 Analyse
CO 3	**Evaluate** the performance of different types of instructions set to write assembly language programs on different software.	HOTS: Level 5 Evaluate
CO 4	**Integrate** knowledge for design of different types of microcontroller based applications through the use of timers & interrupts.	HOTS: Level 6 Create
CO 5	**Create** written records for the given experiments with problem definition, solution, observations & conclusion.	HOTS: Level 6 Create
CO 6	**Demonstrate** ethical practices while performing lab experiments individually or in the group.	LOTS: Level 3 Apply

LIST OF EXPERIMENTS:

1. Write an assembly language program to perform addition & subtraction operation using PIC 16 Microcontroller.
2. Write an assembly language program to perform multiplication and division operation using PIC 16 Microcontroller.
3. Write an assembly language program to perform logical operation using PIC 16 Microcontroller.

4. Write an assembly language program for delay calculation using PIC Microcontroller.
5. Write a program for the blinking of LED's using PIC Microcontroller.
6. Familiarization with Keil software for 8051 & ARM based microcontroller programming.
7. To write and run 8051 assembly language program to perform MUL & DIV operations.
8. Write an assembly language program to add 16 bits using ARM.
9. Write an assembly language program for multiplying two 32 bit numbers using ARM.
10. Write an assembly language program to multiply two matrices using ARM.
11. Write an assembly language program for blinking an LED using Keil and display the result on ARM 7 microcontroller.
12. Write an assembly language program for LCD interfacing using CORTEX ARM microcontroller.

Note: Students are required to perform eight to ten experiments in the semester. The above list is an indicative list of experiments, which can be expanded by course coordinator depending on the course requirement.

Course Articulation Matrix:

Embedded System Design Lab (ECP-718)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	H	L	M	H	H
CO 2	M	L	H	H	H
CO 3	H	M	H	H	H
CO 4	H	M	H	H	H
CO 5	L	H	L	L	L
CO 6	H	M	--	--	--

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective/ Audit	Credit	L
AC01	English For Research Paper Writing	Audit	0	2

Max Marks: 100 (Internal: 30, External: 70)

Course objectives:

This course is introduced to make students understand that how to improve your writing skills and level of readability and learn about what to write in each section. It also imparts the skills needed when writing a title and ensure the good quality of paper at very first-timesubmission.

Unit	Contents	Hours
1	Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness	4
2	Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction	4
3	Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.	4
4	Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,	4
5	Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions	4
6	Useful phrases, how to ensure paper is as good as it could possibly be the first- time submission	4

Text & Reference books:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press Model Curriculum of Engineering & Technology PG Courses [Volume -II] [300].
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht HeidelbergLondon, 2011.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective/ Audit	Credit	L
AC02	Disaster Management	Audit	0	2

Max Marks: 100 (Internal: 30, External: 70)

Course Objective: -

The course aims at the learning to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response. It makes students able to critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives. The course develops an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations. It also provides the ability to critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in.

Units	Contents	Hours
1	**Introduction** Disaster: Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude.	4
2	**Repercussions Of Disasters And Hazards**: Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Manmade disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.	4
3	**Disaster Prone Areas In India** Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics	4
4	**Disaster Preparedness And Management** Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.	4
5	**Risk Assessment** Disaster Risk: Concept And Elements, Disaster Risk Reduction, Global And National Disaster Risk Situation. Techniques Of Risk Assessment, Global Co-Operation In Risk Assessment And Warning, People's Participation In Risk Assessment. Strategies for Survival.	4
6	**Disaster Mitigation** Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation And Non-Structural Mitigation, Programs Of Disaster Mitigation In India.	4

Text & Reference books:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royalbook Company.
2. Sahni, Pardeep Et.Al. (Eds.)," Disaster Mitigation Experiences And Reflections", Prentice Hall Of India,New Delhi.
3. Goel S. L. , Disaster Administration And Management Text And Case Studies" ,Deep & Deep PublicationPvt. Ltd., New Delhi.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective/ Audit	Credit	L
AC04	**Value Education**	**Audit**	**0**	**2**

Max Marks: 100 (Internal: 30, External: 70)

Course Objectives: This course makes students understand value of education and self-development. Imbibe good values in students Model Curriculum of Engineering & Technology PG Courses and let the students know about the importance of character.

Course outcomes:

At the end of the course, students will be able to:

1. Gain knowledge of self-development.
2. Learn the importance of Human values.
3. Develop the overall personality.

Unit	Content	Hours
1	• Values and self-development –Social values and individual attitudes. • Work ethics, Indian vision of humanism. • Moral and non- moral valuation. Standards and principles. • Value judgments	4
2	• Importance of cultivation of values. • Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. • Honesty, Humanity. Power of faith, National Unity. • Patriotism. Love for nature ,Discipline	6
3	• Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline. • Punctuality, Love and Kindness. • Avoid fault Thinking. • Free from anger, Dignity of labour. • Universal brotherhood and religious tolerance. • True friendship. • Happiness Vs suffering, love for truth. • Aware of self-destructive habits. • Association and Cooperation. • Doing best for saving nature	6
4	• Character and Competence –Holy books vs Blind faith. • Self-management and Good health. • Science of reincarnation. • Equality, Nonviolence, Humility, Role of Women. • All religions and same message. • Mind your Mind, Self-control. • Honesty, Studying effectively	6

Text Book:

1. Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford University Press,New Delhi.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective/ Audit	Credit	L
AC07	Stress Management By Yoga	Audit	0	2

Max Marks: 100 (Internal: 30, External: 70)

Course Objectives:

The course aims to achieve overall health of body and mind of the students and emphasizes upon overcoming the stress.

Course Outcomes:

At the end of the course, students will be able to:

1. Develop healthy mind in a healthy body thus improving social health also.
2. Improve efficiency.

Unit	Content	Hours
1	• Definitions of Eight parts of yog. (Ashtanga)	8
2	• Yam and Niyam. Do`s and Don't's in life. i. Ahinsa, satya, astheya, bramhacharya and aparigraha ii. Shaucha, santosh, tapa, swadhyay, ishwarpranidhan	8
3	• Asan and Pranayam i. Various yog poses and their benefits for mind & body ii. Regularization of breathing techniques and its effects-Types of pranayam	8

Text and Reference books:

1. "Yogic Asanas for Group Tarining-Part-I" : Janardan Swami Yogabhyasi Mandal, Nagpur.
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (PublicationDepartment), Kolkata.

Second Semester

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective	Credit	L	P
ECL-721	Mobile Communication	Core	4	4	0

Max Marks: 100 (Internal: 30, External: 70)

Course Assessment Methods: Both Continuous & Semester End Assessment

Pre-requisites: Communication System

Course Objectives:

This course is introduced to develop basic understanding and impart in-depth knowledge of various concepts used in wireless mobile communication. The course imparts the concepts, parameters & models of mobile radio propagation also helps students understand the architecture and elements of wireless standards and systems like GSM, GPRS, CDMA, etc. It also provides coverage to the advanced, latest and upcoming wireless technologies like OFDM, Multicarrier Modulation, 4G, 5G, turbo codes and multi-user detection etc.

Course Outcomes:

Sr. No.	At end of the semester, students will be able to	RBT Level
CO-1	**Describe** terminologies & various generations of wireless communication systems and there technical specifications.	LOTS: Level 1 Remember
CO-2	**Understand** the concepts of cellular system, fading, multiple access techniques and multicarrier systems.	LOTS: Level 2 Understand
CO-3	**Apply** the concepts of radio planning for cellular mobile communication systems.	LOTS: Level 3 Apply
CO-4	**Analyze & evaluate** the performance of various wireless communication systems.	HOTS: Level 4 & 5 Analyze & evaluate
CO-5	**Design** basic wireless communication system in a better fashion with thorough knowledge of wireless communication technologies.	HOTS: Level 6 Create

UNIT-1

Introduction to Wireless Communication Systems: Various Generations of wireless mobile communication from 1G to 5G, The Cellular Concept, Frequency reuse, channel assignment strategies, hand-off strategies, interference and system capacity, improving capacity of cellular system through cell splitting, sectoring, etc.

UNIT-2

Mobile Radio Propagation: Introduction to radio wave propagation, three basic propagation mechanisms, Outdoor & indoor propagation models, small scale multipath propagation, parameters of mobile multipath channel, small scale & large scale fading, their types. **Wireless Systems:** Basic architecture of GSM, GPRS, 3G, 4G & 5G.

UNIT-3

CDMA System Concepts: Basics of CDMA. Spread spectrum concept. time hopping, Direct Sequence and Frequency Hopped Spread Spectrum, Chirp spread spectrum systems, Hybrid systems, Spreading sequences and their correlation functions, Code generation, Properties and generation of PN sequences, RAKE receiver, Diversity techniques an Rake receiver, Soft handoffs.

UNIT-4

Implementation Issues: OFDM, Multi-Carrier Modulation and Demodulation, Introduction to MIMO systems, Channel Coding and Decoding (Convolutional codes, Turbo codes), Multi-user Detection: Decorrelating detector, MMSE detector. Successive Interference Canceller, Parallel Interference Canceller.

Text Books:

1. Mobile Cellular Telecommunications; 2nd ed.; William, C Y Lee McGraw Hill
2. Wireless and Digital Communications; Dr. KamiloFeher (PHI)
3. Principles of Mobile Communication, G.L Stuber Kluwer Academic, 1996
4. Wireless Communication; Principles and Practice; T.S.Rappaport

Note: The Examiner will set nine questions. First question will be compulsory, covering the entire syllabus. Apart from Question No. 1, rest of the paper will consist of four units as per the syllabus taking two questions from each unit. However, student may be asked to attempt only 1 question from each unit. All questions will carry equal marks.

Course Articulation Matrix:

Mobile Communication (ECL-721)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	M	--	H	H	M
CO 2	M	--	H	H	H
CO 3	H	L	H	M	H
CO 4	H	--	H	H	H
CO 5	H	M	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective	Credit	L	P
ECL-722	Advance Optical Communication System	Core	4	4	0

Max Marks: 100 (Internal: 30 External: 70)

Course Assessment Methods: Both Continuous & Semester End Assessment

Pre-requisites: Physics of optical communication components and applications to communication systems

Course Objectives:

This course deals with the understanding of the optical components and the design and operation of optical fiber communication systems. The principles of wavelength division multiplexed (WDM) systems, SONET, SDH and passive optical networks. The characteristics and limitations of system components (laser diodes, external modulators, optical fiber, optical amplifiers, optical receivers) and the factors affecting the performance of the optical communication system.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able to	RBT Level
CO 1	**Describe** the fundamentals and components of optical communication system.	LOTS: Level 1 Remember
CO 2	**Understand** the channel impairments, optical sources, detectors and non linearities etc. in optical communication system.	LOTS: Level 2 Understand
CO 3	**Apply** the fundamentals of optical communication for design of optical communication link as well as system.	LOTS: Level 3 Apply
CO 4	**Analyze and evaluate** the performance of various optical communication systems.	HOTS: Level 4 & 5 Analyze & evaluate
CO 5	**Design** optical fiber communication links using appropriate optical components.	HOTS: Level 6 Create

UNIT-1

Review: Evolution of Basic Fiber Optic Communication System, Benefits and disadvantages of Fiber Optics, Transmission Windows, Transmission Through Optical Fiber, The Numerical Aperture (NA), The Optical Fiber, Types of Fiber, Different Losses & Issues in Fiber Optics, Attenuation in Optical Fibers, Fiber Optic Loss Calculations, Dispersion, connectors & splices, bending loses, Absorption, scattering, very low loss materials, plastic & polymer-clad-silica fibers. Wave propagation in step index & graded index fiber, fiber dispersion, single mode fibers, multimode fibers, dispersion shifted fiber, dispersion flattened fiber, polarization, cut-off condition and V-parameter.

UNIT-2

Fiber Optic System Design Considerations and Components: Indoor Cables, Outdoor Cables, Cabling Example, Power Budget, Bandwidth and Rise Time Budgets, Electrical and Optical Bandwidth, Connectors, Fiber Optic Couplers.

Dispersion and Nonlinearities Dispersion in single mode and multimode fibers, dispersion shifted and dispersion flattened fibers, attenuation and dispersion limits in fibers, Kerr nonlinearity, self phase modulation, Cross Phase Modulation, FWM.

UNIT-3

Optical Sources: optical source properties, operating wavelength of optical sources, semiconductor light-emitting diodes and laser diodes, semiconductor material and device operating principles, light-emitting diodes, surface-emitting LEDS, edge-emitting LEDS, super luminescent diodes, laser diodes, comparison of LED and ILD. Fiber optic transmitters, basic optical transmitters, direct versus external modulation, fiber optic transmitter applications.

Optical Detectors: Basic Information on light detectors, Role of an optical detector, Detector characteristics: Responsivity, Noise Equivalent Power, Detectivity, Quantum efficiency, The PN junction photo diode - PIN photodetectors - Avalanche photo diode construction characteristics and properties, APD Specifications, Applications of APD, Optical Receivers .

UNIT-4

Advanced Multiplexing Strategies: Optical TDM, subscriber multiplexing (SCM), WDM and Hybrid multiplexing methods.

Optical Networking: Data communication networks, network topologies, MAC protocols, Network Architecture- SONET/TDH, optical transport network, optical access network, optical premise network.

Text Books:

1. G.P Aggrawal, Fiber-Optic Communication Systems, Wiley-interscience.
2. G. Keiser, Optical Fiber Communication, Tata –McGraw Hill.
3. John Gowar , Optical communication systems, PHI.

Note: The Examiner will set nine questions. First question will be compulsory, covering the entire syllabus. Apart from Question No. 1, rest of the paper will consist of four units as per the syllabus taking two questions from each unit. However, student may be asked to attempt only 1 question from each unit. All questions will carry equal marks.

Course Articulation Matrix:

Advance Optical Communication System (ECL-722)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	H	--	M	H	M
CO 2	H	--	M	H	M
CO 3	H	--	M	H	M
CO 4	M	--	H	H	H
CO 5	M	--	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective	Credit	L	P
ECL-723	Analog IC Design	Core	4	4	0

Max Marks: 100 (Internal: 30, External: 70)

Course Assessment Methods: Both Continuous & Semester End Assessment

Pre-requisites: Introduction to microelectronics circuits including bipolar and MOS transistors

Course Objectives:

This Course is for the First year post-graduate students. The pre-requisite for the course is basic knowledge of semiconductor devices and an introduction to analog electronics. This course covers the design and analysis of various linear and non-linear analog circuits like amplifiers, current mirrors, comparators, oscillators, phase-locked loops etc. using both bipolar and MOS transistors. Various design parameters are covered.

Course Outcomes:

Sr. No.	At end of the semester, student will be able to	RBT Level
CO-1	**Describe** CMOS technologies for analog IC design.	LOTS: Level 1 Remember
CO-2	**Understand** analog CMOS circuits, systems and their uses.	LOTS: Level 2 Understand
CO-3	**Apply** the concepts of analog circuit design for the implementation of CMOS based integrated circuits and systems.	LOTS: Level 3 Apply
CO-4	**Analyze & evaluate** large and small signal behaviour of analog circuits.	HOTS: Level 4 & 5 Analyze & evaluate
CO-5	**Design** analog CMOS circuits and systems.	HOTS: Level 6 Create

UNIT-1

Introduction to Analog Design, integrated circuits, CMOS Technology: brief history, levels of abstraction, robust analog design, basic MOS device physics-transistor and switch, MOS structure, MOSFET current voltage characteristics, second order effects, MOS models-small signal and large signal model, MOS capacitances, MOS SPICE model

UNIT- 2

Single stage amplifiers-common source, CS with resistive load, CS with diode connected load, CS with current source, CS triode load stage, CS with source degeneration, source follower, common gate, cascode stage, Differential amplifier, basic differential pair, common mode response, differential pair with MOS loads, DC transfer characteristics.

UNIT- 3

Basic MOS current mirrors, cascode current mirror, Wilson current mirror, widlar current mirror, voltage references, general considerations, supply independent biasing, temperature independent references, Operational Amplifier: Applications of operational Amplifier, theory and Design; Definition of Performance Characteristics; Design of one and two stage MOS Operational Amplifier, two stage MOS operational Amplifier with cascodes, MOS Folded-cascode operational amplifiers, Frequency response & compensation.

UNIT- 4

Nonlinear Analog Circuits: CMOS Comparators, Phase Locked Loops (PLL), closed loop analysis of PLL and applications. Voltage controlled oscillator, Digital-to-Analog (D/A) and Analog-to-Digital (A/D) Converters, Operational transconductance Amplifier (OTA), Switched Capacitor circuits.

Text Books:

1. Paul R. Gray, Paul J. Hurst, Stephen Lewis, and Robert G Meyer, "Analysis and Design of Analog Integrated Circuits", 5th Edition Wiley, 2014
2. Behzad Razavi, Design of Analog CMOS Integrated Circuits, Indian Edition, McGraw Hill Education, 2014

Reference Books:

1. R Gregorian and G C Temes, Analog MOS Integrated Circuits for Signal Processing, John Wiley, 1986.
2. D. A. Johns and Martin, Analog Integrated Circuit Design, John Wiley, 1997.
3. BehzadRazavi, "Principles of data conversion system design", S.Chand and company Ltd, 2000. John Wiley
4. Kenneth R. Laker, Willy M.C. Sensen, "Design of Analog Integrated circuits and systems", McGraw Hill, 1994.

Note: The Examiner will set nine questions. First question will be compulsory, covering the entire syllabus. Apart from Question No. 1, rest of the paper will consist of four units as per the syllabus taking two questions from each unit. However, student may be asked to attempt only 1 question from each unit. All questions will carry equal marks.

Course Articulation Matrix:

Analog IC Design (ECL-723)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	H	L	H	H	H
CO 2	H	L	M	H	L
CO 3	M	L	H	H	M
CO 4	M	L	H	H	M
CO 5	M	L	H	H	M

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective	Credit	L	P
ECL-724	Adaptive Signal Processing	Core	4	4	0

Max marks: 100 (Internal: 30, External: 70)

Course Assessment Methods: Both Continuous & Semester End Assessment

Pre-requisites: Signals and Systems, Digital Signal Processing

Course Objectives:

To introduce the concepts and techniques associated with the understanding of digital signal processing. To familiarize with techniques suitable for analyzing and synthesizing both continuous-time and discrete time systems. To provide with an appreciation of applications for the techniques and mathematics used in this course.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able to:	RBT Level
CO-1	**Define & describe** the significance of signal processing in the fields of computing and telecommunications.	LOTS: Level 1 Remember
CO-2	**Understand & explain** various digital filters used in signal processing.	LOTS: Level 2 Understand
CO-3	**Apply** adaptive algorithm for the analysis of adaptive filtering application	LOTS: Level 3 Apply
CO-4	**Analyze & evaluate** various models for adaptive filtering application	HOTS: Level 4 & 5 Analyze & evaluate
CO-5	**Design** various types of filter used in signal processing.	HOTS: Level 6 Create

UNIT-1

Basic of Digital Signal Processing: Signals and Information, Signal Processing Methods, Applications of Digital Signal Processing, Derivation of the z-Transform Properties of z-Transform, Fourier series and Fourier transform. Random variable, Stochastic processes.

UNIT-2

Design of Digital Filters: Introduction, Linear Time-Invariant Digital Filters, Recursive and Non-Recursive Filters, Filtering Operation, Sum of Vector Products, A Comparison of Convolution and Correlation, Filter Structures, Direct, Cascade and Parallel Forms, Linear Phase FIR Filters Design of Digital FIR Filter-banks, Sub-band Filters, Design of Infinite Impulse Response IIR filters, Issues in the Design and Implementation of a Digital Filter.

UNIT-3

Adaptive Filtering: introduction to random process, Basic of adaptive filtering. Performance function, factors determining the choice of algorithm, method of Steepest-Descent, LMS algorithm, modified LMS algorithm, Normalized LMS algorithm, important properties of LMS, implementation consideration, Computational issues.

UNIT-4

Adaptive Filter Applications: Adaptive echo cancellation, Principle of adaptive echo cancellation, Sub band acoustic echo cancellation, echo cancellation with linear prediction pre whitening, Stereophonic echo cancellation Performance evaluation of echo canceller, Adaptive noise cancellation, Adaptive line enhancer.

Text Books:

1. Simon S Haykins, "Adaptive Filter Theory," PHI, 3rd Edition
2. Proakis, "Digital Signal Processing," PHI 2nd edition
3. Harry L. Van Trees, "Detection, Estimation, and Modulation Theory, Part 1&3," Wiley 2002
4. Saeed V. Vaseghi, "Advanced Digital Signal Processing and Noise Reduction," Third Edition,2006
5. Eberhard Hänsler, "Gerhard Schmidt Acoustic Echo and Noise Control: A Practical Approach," wiley, 2005.

Note: The Examiner will set nine questions. First question will be compulsory, covering the entire syllabus. Apart from Question No. 1, rest of the paper will consist of four units as per the syllabus taking two questions from each unit. However, student may be asked to attempt only 1 question from each unit. All questions will carry equal marks.

Course Articulation Matrix:

Adaptive Signal Processing (ECL-724)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	--	--	M	H	M
CO 2	L	L	H	M	H
CO 3	L	--	M	H	H
CO 4	M	L	M	H	H
CO 5	M	L	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective	Credit	L	P
ECL-725(i)	Algorithm for VLSI Design Automation	Elective	4	4	0

Max Marks: 100 (Internal: 30, External: 70)

Course Assessment Methods: Both Continuous & Semester End Assessment

Pre-requisites: VLSI Design

Course Objectives:
This course is for first year post graduation students. This course is designed to demonstrate the use of data structure to build up the CAD tools for simulation, synthesis and physical VLSI design.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able:	RBT Level
CO 1	**Define & describe** the terminology and fundamental principles related to VLSI design automation.	LOTS: Level 1 Remember
CO 2	**Understand & explain** logic synthesis, VLSI automation algorithms, routing algorithms, VLSI compaction.	LOTS: Level 2 Understand
CO 3	**Apply** the various VLSI automation algorithms for high-level synthesis.	LOTS: Level 3 Apply
CO 4	**Analyze & evaluate** the significance of VLSI automation algorithms, routing algorithms, via minimization and VLSI compaction.	HOTS: Level 4 & 5 Analyze and Evaluate
CO 5	**Design & develop** hardware models for VLSI design based applications.	HOTS: L6 Create

UNIT-1

Logic synthesis & verification:
Introduction to combination all logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.

UNIT-2

VLSI automation Algorithms:
Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

Placement, floor planning & pin assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint-based floor planning, floor planning algorithms for mixed block &cell design. General & channel pin assignment.

Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches.

UNIT-3

Detailed routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switch box routing algorithms.

UNIT-4

Over the cell routing & via minimization: two layers over the cell routers, constrained &unconstrained via minimization.

Compaction: problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction

Text Books:

1. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.

Reference Books:

1. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.
2. Rolf Drechsheler "Evolutionary Algorithm for VLSI", Second edition
3. Trimburger, "Introduction to CAD for VLSI", Kluwer Academic publisher, 2002

Note: The Examiner will set nine questions. First question will be compulsory, covering the entire syllabus. Apart from Question No. 1, rest of the paper will consist of four units as per the syllabus taking two questions from each unit. However, student may be asked to attempt only 1questionfrom each unit. All questions will carry equal marks.

Course Articulation Matrix:

Algorithm for VLSI Design Automation (ECL-725(i))					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	M	--	H	H	M
CO 2	H	--	H	H	M
CO 3	H	L	H	H	H
CO 4	H	L	H	H	H
CO 5	H	M	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective	Credit	L	P
ECL-725(ii)	Advanced Computer Architectures	Elective	4	4	0

Max Marks: 100 (Internal: 30, External: 70)

Course Assessment Methods: Both Continuous & Semester End Assessment

Pre-requisites: Basics of digital electronics and computer organization

Course Objectives:

Understand the architecture of a modern computer with its various processing units and the performance measurement of the computer system. The course also provides knowledge about memory management system of computer.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able to:	RBT Level
CO 1	**Define& describe** the terminology and fundamental principles related to advanced computer architectures.	LOTS: Level 1 Remember
CO 2	**Understand & explain** parallel computer models, advanced/multiprocessor architecture, memory designs/architecture.	LOTS: Level 2 Understand
CO 3	**Demonstrate** computer models and architecture, network properties, memory organizations and architecture.	LOTS: Level 3 Apply
CO 4	**Analyze & evaluate the significance of pipelining, interconnections, memory hierarchy organizations and protocols.**	HOTS: Level 4 & 5 Analyze and Evaluate
CO 5	**Design** memory hierarchy, static and dynamic interconnection networks.	HOTS: L6 Create

UNIT-1

Parallel computer models: The state of computing, Classification of parallel computers, Multiprocessors and multi computers, Multivector and SIMD computers.
Program and network properties: Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms

UNIT-2

System Interconnect Architectures: Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network.
Advanced processors: Advanced processor technology, Instruction- set Architectures, CISC

Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors Pipelining: Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, b ranch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines.

UNIT-3

Memory Hierarchy Design: Cache basics & cache performance, reducing miss rate and miss penalty, multi level cache hierarchies, main memory organizations, design of memory hierarchies.

Multiprocessor architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenge of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, synchronization.

UNIT-4

Scalable point –point interfaces: Alpha364 and HT protocols, high performance signaling layer.

Enterprise Memory subsystem Architecture: Enterprise RAS Feature set: Machine check, hot add/remove, domain partitioning, memory mirroring/migration, patrol scrubbing, fault tolerant system.

Text Books:

1. Kai Hwang, "Advanced computer architecture";TMH.
2. D.A. Patterson, "Computer organization and design,"MorganKaufmann,2nd Ed.

References:

1. J.P.Hayes, "Computer Architecture and organization"; MGH.
2. Harvey G.Cragon, "Memory System and Pipelined processors"; Narosa Publication.
3. V.Rajaranam & C.S.R.Murthy,"Parallel computer";PHI.
4. R.K.Ghose, Rajan Moona & Phalguni Gupta, "Foundation of Parallel Processing" Narosa Publications.
5. Kai Hwang and Zu, "Scalable Parallel Computers Architecture"; MGH.
6. Stalling W, "Computer Organisation & Architecture"; PHI.
7. D.Sima, T. Fountain, P. Kasuk, "Advanced Computer Architecture- Design space Approach,"AddisonWesley,1997.
8. M.J Flynn, "Computer Architecture, Pipelined and Parallel Processor Design"; Narosa Publishing.
9. D.A.Patterson, J.L.Hennessy," Computer Architecture: A quantitative approach"; Morgan Kauffmann feb,2002.
10. Hwan and Briggs, "Computer Architecture and Parallel Processing"; MGH.VLSI

Note: The Examiner will set nine questions. First question will be compulsory, covering the entire syllabus. Apart from Question No. 1, rest of the paper will consist of four units as per the syllabus taking two questions from each unit. However, student may be asked to attempt only 1questionfrom each unit. All questions will carry equal marks.

Course Articulation Matrix:

Advanced Computer Architectures (ECL-725(ii))					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	M	--	H	H	M
CO 2	M	--	H	H	H
CO 3	H	L	M	H	H
CO 4	H	L	H	H	H
CO 5	H	M	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective	Credit	L	P
ECL-725 (iii)	MEMS & IC Integration	Elective	4	4	0

Max Marks: 100 (Internal: 30, External: 70)

Course Assessment Methods: Both Continuous & Semester End Assessment
Pre-requisites: IC fabrication techniques, Analog & Digital VLSI design.

Course Objectives:
This course has been developed due to industry request and as an introduction to a growing and important field in our high technology future. The objectives of this course are to teach critical thinking in micro engineering process, materials and design issues, to build an understanding of micro scale physics for use in designing MEMS applications, review current MEMS, RFMEMS and Bio MEMS applications, use the above knowledge to design and fabricate novel EMS/Bio MEMS /RF MEMS applications as part of a group project.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able to:	RBT Level
CO-1	**Define & Describe** the terminologies used in MEMS & IC fabrication.	LOTS: Level 1 Remember
CO-2	**Understand & explain** basic approach to various micro-sensors, micro-actuators, their types and applications.	LOTS: Level 2 Understand
CO-3	**Apply** their understanding in fabrication process and characterization of MEMS & ICs.	LOTS: Level 3 Apply
CO-4	**Analyze & evaluate** the performance of MEMS devices and ICs based on their characterization results.	HOTS: Level 4 & 5 Analyze & evaluate
CO-5	**Design** various simple micro-devices, micro-systems using MEMS and ICs fabrication techniques.	HOTS: Level 6 Create

UNIT-1

MEMS Fabrication: Conventional MEMS fabrication using VLSI technology: lithography, chemical etching: isotropic and anisotropic, Plasma etching, Reactive ion etching, Oxidation, Chemical vapor deposition, LPCVD, PECVD, Surface micromachining, LIGA, single layer and higher layer fabrication, Non-conventional MEMS fabrication: laser micromachining and welding micromachining(EDM & ECM), dynamic mask process, Electronic packaging.

UNIT-2

MEMS Sensors: Physical Micro Sensors: Classification of physical sensors, Integrated, Intelligent, or Smart Sensors. Sensing mechanisms: Piezoresistive sensing, Capacitive sensing, Piezoelctric sensing, Resonant sensing. Interdigital Transducer (IDT) and Surface Acoustic Waves (SAW) sensor. Microactuation: Electrostatic Actuation, Magnetic Actuation, Piezoelectric Actuation, Thermal Actuation.

UNIT-3

MEMS Design & Analysis: Basic concepts of design of MEMS devices and processes, Design for fabrication, Other design considerations, Analysis of MEMS devices, Modeling and Simulation.

UNIT-4

MEMS Characterization: Technologies for MEMS characterization, Scanning Probe Microscopy (SPM), Atomic Force Microscopy (AFM), Scanning Tunneling Microscopy (STM), Magnetic Force Microscopy, Scanning Electron Microscope.

Text Books:

1. Gregory T.A. Kovacs, Micro machined Transducers Source book, The McGraw-Hill, Inc. 1998
2. Stephen D. Senturia, Microsystem Design, Kluar Publishers, 2001
3. Nadim Maluf, An Introduction to Microelectromechanical Systems Engineering, Artech House, 2000.
4. Masood Tabib-Azar, Microactuators, Kluwer, 1998.
5. H. J. De Los Santos, Introduction to Microelectromechanical (MEM) Microwave Systems, Artech, 1999.

Note: The Examiner will set nine questions. First question will be compulsory, covering the entire syllabus. Apart from Question No. 1, rest of the paper will consist of four units as per the syllabus taking two questions from each unit. However, student may be asked to attempt only 1 question from each unit. All questions will carry equal marks.

Course Articulation Matrix:

MEMS & IC Integration (ECL-725 (iii))					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	M	L	H	H	H
CO 2	H	L	H	H	H
CO 3	H	--	H	H	H
CO 4	H	L	H	H	H
CO 5	H	--	H	H	H

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective	Credit	L	P
ECP-726	Adaptive Signal Processing Lab	Core	2	0	4

Max Marks: 100 (Internal: 30, External: 70)

Course Assessment Methods: Both Continuous & Semester end assessment

Pre-requisites: Basic of MATLAB, Concept of digital signal processing and adaptive digital signal processing.

Course Objectives:

This course is designed to demonstrate the use of MATLAB and other open source software for simulation, synthesis and designing of different processing systems. Apart from this working with the DSP processor hardware is familiarized.

Course Outcomes:

Sr. No.	At the end of the semester, students will be able to:	RBT Level
CO-1	**Understand software** tools and apply these tools for the realization of various filter designs.	LOTS: Levels 3 Apply
CO-2	**Analyze and compare** the outcomes of different experimental models.	HOTS: Level 4 Analyze
CO-3	**Evaluate** the performance of different windowing techniques to design various filters.	HOTS: Level 5 Evaluate
CO-4	**Integrate** knowledge for design of various tools and commands for interference cancellation and direction of arrival	HOTS: Level 6 Create
CO-5	**Create** written records for the given experiments with problem definition, solution, observations & conclusion.	HOTS: Level 6 Create
CO-6	**Demonstrate** ethical practices while performing lab experiments individually or in the group.	LOTS: Level 3 Apply

List of Experiments:

1. To write Matlab statement for Algebraic Equations.
2. To write a program for adaptive filter application in interference cancellation.
3. To write a program for Direction of arrival estimation.
4. To write a program for filter design with the help of Matlab filter design tool.
5. To write a program for designing filters from Windowing techniques.

6. To write a program for to find the Power spectral Density.
7. To simulate the given model using simulink tool.
8. To write a program for cross correlation and auto correlation.
9. To familiarize with working of DSP Processor & Hardware.

Note: Students are required to perform eight to nine experiments in the semester. The above list is an indicative list of experiments, which can be expanded by course coordinator depending on the course requirement.

Course Articulation Matrix:

Adaptive Signal Processing Lab (ECP-726)					
	PO 1	**PO 2**	**PO 3**	**PSO 1**	**PSO 2**
CO 1	M	M	M	H	H
CO 2	M	L	M	H	H
CO 3	H	M	M	H	H
CO 4	M	L	M	H	H
CO 5	L	H	L	L	L
CO 6	H	M	--	--	--

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective/ Audit	Credit	L
AC03	Sanskrit For Technical Knowledge	Audit	0	2

Max Marks: 100 (Internal: 30, External: 70)

Course Objectives:

The course is aimed To get a working knowledge in illustrious Sanskrit, the scientific language in the world as Learning of Sanskrit to improve brain functioning. It helps to develop the logic in mathematics, science & other subjects enhancing the memory power. The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from the ancient literature.

Course Outcomes:

Students will be able to

1. Understanding basic Sanskrit language.
2. Ancient Sanskrit literature about science & technology can be understood.
3. Being a logical language will help to develop logic in students.

Unit	Content	Hours
1	• Alphabets in Sanskrit, • Past/Present/Future Tense, • Simple Sentences	8
2	• Order • Introduction of roots • Technical information about Sanskrit Literature	8
3	• Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics	8

Text & Reference Books:

1. "Abhyaspustakam" – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi.
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam,New Delhi Publication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective/ Audit	Credit	L
AC05	Constitution Of India	Audit	0	2

Max Marks: 100 (Internal: 30, External: 70)

Course Objectives:

The course is introduced to make students understand the premises informing the twin themes of liberty and freedom from a civil rights perspective. It helps to address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism. The course also addresses the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 andits impact on the initial drafting of the Indian Constitution.

Course Outcomes: Students will be able to:

1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival ofGandhi in Indian politics.
2. Discuss the intellectual origins of the framework of argument that informed the conceptualization of socialreforms leading to revolution in India.
3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adultsuffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of 1956.

Units	Content	Hours
1	• **History of Making of the Indian Constitution:** History Drafting Committee, (Composition & Working)	4
2	• **Philosophy of the Indian Constitution:** Preamble Salient Features	4
3	• **Contours of Constitutional Rights & Duties:** ▪ Fundamental Rights ▪ Right to Equality ▪ Right to Freedom ▪ Right against Exploitation ▪ Right to Freedom of Religion ▪ Cultural and Educational Rights ▪ Right to Constitutional Remedies ▪ Directive Principles of State Policy ▪ Fundamental Duties.	4

4	• **Organs of Governance:** ▪ Parliament ▪ Composition ▪ Qualifications and Disqualifications ▪ Powers and Functions ▪ Executive ▪ President ▪ Governor ▪ Council of Ministers ▪ Judiciary, Appointment and Transfer of Judges, Qualifications ▪ Powers and Functions	4
5	• **Local Administration:** ▪ District's Administration head: Role and Importance,	4
	▪ Municipalities: Introduction, Mayor and role of Elected representative, CEO of Municipal Corporation. ▪ Pachayati raj: Introduction, PRI: Zila Pachayat. ▪ Elected officials and their roles, CEO Zila Pachayat: Position and role. ▪ Block level: Organizational Hierarchy (Different departments), ▪ Village level: Role of Elected and Appointed officials, ▪ Importance of grass root democracy	
6	• **Election Commission:** ▪ Election Commission: Role and Functioning. ▪ Chief Election Commissioner and Election Commissioners. ▪ State Election Commission: Role and Functioning. ▪ Institute and Bodies for the welfare of SC/ST/OBC and women.	4

Text & Reference Books:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective/ Audit	Credit	L
AC06	Pedagogy Studies	Audit	0	2

Max Marks: 100 (Internal: 30, External: 70)

Course Objectives:

The course helps students to review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers. It also helps to identify critical evidence gaps to guide the development.

Course Outcomes: Students will be able to understand:

1. What pedagogical practices are being used by teachers in formal and informal classrooms in developingcountries?
2. Model Curriculum of Engineering & Technology PG Courses [Volume -II] [306]
3. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with whatpopulation of learners?
4. How can teacher education (curriculum and practicum) and the school curriculum and guidance materialsbest support effective pedagogy?

Units	Content	Hours
1	• **Introduction and Methodology:** ▪ Aims and rationale, Policy background, Conceptual framework and ▪ terminology ▪ Theories of learning, Curriculum, Teacher education. ▪ Conceptual framework, Research questions. ▪ Overview of methodology and Searching.	4
2	▪ Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. ▪ Curriculum, Teacher education.	2
3	▪ Evidence on the effectiveness of pedagogical practices ▪ Methodology for the in depth stage: quality assessment of included studies. ▪ How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? ▪ Theory of change. ▪ Strength and nature of the body of evidence for effective pedagogical practices. ▪ Pedagogic theory and pedagogical approaches. ▪ Teachers' attitudes and beliefs and Pedagogic strategies.	4
4	▪ Professional development: alignment with classroom practices and follow-up support ▪ Peer support ▪ Support from the head teacher and the community. ▪ Curriculum and assessment ▪ Barriers to learning: limited resources and large class sizes	4

5	• **Research gaps and future directions** ▪ Research design ▪ Contexts ▪ Pedagogy ▪ Teacher education ▪ Curriculum and assessment ▪ Dissemination and research impact.	2

Text & Reference Books:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational development, 33(3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course code	Title of course	Core/Elective/ Audit	Credit	L
AC08	**Personality Development ThroughLife Enlightenment Skills**	**Audit**	**0**	**2**

Max Marks: 100 (Internal: 30, External: 70)

Course Objectives:
This course helps students to learn to achieve the highest goal happily. To become a person with stable mind, pleasing personality and determination. To awaken wisdom in students

Course Outcomes: Students will be able to:
1. Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve thehighest goal in life.
2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity.
3. Study of Neetishatakam will help in developing versatile personality of students.

Unit	Content	Hours
1	Neetisatakam-Holistic development of personality • Verses- 19,20,21,22 (wisdom) • Verses- 29,31,32 (pride & heroism) • Verses- 26,28,63,65 (virtue) • Verses- 52,53,59 (dont's) • Verses- 71,73,75,78 (do's)	8
2	• **Approach to day to day work and duties.** • **Shrimad Bhagwad Geeta : Chapter 2-Verses 41, 47,48,** • **Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35,** • Chapter 18-Verses 45, 46, 48.	8
3	• Statements of basic knowledge. • **Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68** • **Chapter 12 -Verses 13, 14, 15, 16,17, 18** • **Personality of Role model. Shrimad Bhagwad Geeta: Chapter2-Verses 17, Chapter 3-Verses 36,37,42,** • Chapter 4-Verses 18, 38,39 • Chapter18 – Verses 37,38,63	8

Text & Reference Books:

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, NewDelhi.